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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,831	01/23/2002	Bin Liu	STL10077	1548

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EXAMINER	
CHASE, SHELLY A	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,831	LIU ET AL.	
	Examiner	Art Unit	
	Shelly A Chase	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-24* is/are allowed.

6)☒ Claim(s) *1-5,25-27 and 29* is/are rejected.

7)☒ Claim(s) *6-10 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-23-2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 23 are presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 1-23-2002 have been considered by examiner (see attached PTO-1449).

Claim Objections

3. Claims 11 and 19 are objected to because of the following informalities: please change "the estimated codewords" to --- estimated codewords ----, recited on line 13 and revise " where the second decoding uses the same error correction circuit as the first decoding" recited on lines 15 to 16. The phrase on lines 15 to 16 is confusing since; the claim states that the error correction circuit is designed to perform a first decoding and a second decoding. Claim 19 has a similar problem.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20, recites the limitation "the single burst error correction" recited on line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 17 has a similar problem.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claim **25** is rejected under 35 U.S.C. 102(e) as being anticipated by Kelly (USP 6557126 B1).

Claim **25**:

Kelly teaches an apparatus for determining the write power in an optical disk utilizing cross interleave Reed Solomon (CIRC) technique, the apparatus comprising a CIRC encoder (see fig. 9 and col. 8, lines 62 et seq.), and a CIRC decoder decoding the interleaved encoded codeword (see fig. 10 and col. 9, lines 35 to 40) wherein the decoder set erasure flags for uncorrected errors (see col. 9, lines 50 to 55).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 to are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly in view of Yi et al. (*interleaving and decoding scheme for a product code for a mobile data communication*, IEEE).

Claim **1**:

Kelly substantially teaches the claimed invention. Kelly teaches an apparatus for determining the write power in an optical disk utilizing cross interleave Reed Solomon (CIRC) technique. The apparatus comprising a CIRC decoder (see fig. 1), the decoder comprising: a delay circuit [214] ("de-interleaver") receiving the interleaved encoded codeword (see col. 9, lines 35 to 41). Kelly also teaches that the decoder comprises a C1 decoder [216] performing decoding on the received codeword from the delay circuit

(see col. 9, lines 42 to 46) and the C1 decoder set an erasure flag for the uncorrected errors (see col. 9, lines 50 to 55).

Kelly further teaches that the decoder includes a C2 decoder [222] performing decoding on the received de-interleave block [220], which has the C1 erasure flag marking (see col. 10, lines 1 to 10). Kelly teaches that C1 and C2 coding are Reed Solomon coding (see col. 8, lines 65 to 66) and the C2 decoding correct errors according to the erasure flag (see col. 10, lines 10 to 20).

Kelly does not specifically teach that the interleaved codewords was done in such a manner that any *L* consecutive symbols consist of exactly one symbol from each of the *L* codewords; however, Yi in an analogous art teaches interleaving and decoding for a product code wherein diagonal interleaving is performed and two symbols in the same row become $\mathbf{n_2}$ symbols apart (see pg. 145 par. 1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the interleaving process of Kelly to include diagonal interleaving as taught by Yi. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a diagonal interleaver for improved performance as taught by Yi (see abstract).

As per claims **2** and **3**, Kelly teaches that the C2 decoder receives the de-interleaved C1 decoded symbol and for each symbol provides indication if the symbol is unreliable and the C2 decoder decoding according to the received erasure flag (see col. 10, lines 4 to 24); interpreted as marking erasure position according to error positions extracted from correctable estimated codewords.

As per claims **4** and **5**, Kelly teaches that both C1 and C2 decoders set erasure flags for uncorrectable errors (see col. 10, lines 7 et seq.).

Claim **26, 27** & **29**:

Kelly substantially teaches the claimed invention. Kelly teaches an apparatus for determining the write power in an optical disk utilizing cross interleave Reed Solomon (CIRC) technique. The apparatus comprising a CIRC decoder (see fig. 1), the decoder comprising: a delay circuit [214] ("de-interleaver") receiving the interleaved encoded codeword (see col. 9, lines 35 to 41). Kelly also teaches that the decoder comprises a C1 decoder [216] performing decoding on the received codeword from the delay circuit (see col. 9, lines 42 to 46) and the C1 decoder set an erasure flag for the uncorrected errors (see col. 9, lines 50 to 55).

Kelly further teaches that the decoder includes a C2 decoder [222] performing decoding on the received de-interleave block [220], which has the C1 erasure flag marking (see col. 10, lines 1 to 10). Kelly teaches that C1 and C2 coding are Reed Solomon coding (see col. 8, lines 65 to 66) and the C2 decoding correct errors according to the erasure flag set by the C1 decoder (see col. 10, lines 10 to 20).

Kelly does not specifically teach that the interleaved codewords was done in such a manner that any *L* consecutive symbols consist of exactly one symbol from each of the *L* codewords; however, Yi in an analogous art teaches interleaving and decoding for a product code wherein diagonal interleaving is performed and two symbols in the same row become $\mathbf{n_2}$ symbols apart (see pg. 145 par. 1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made

to modify the interleaving process of Kelly to include diagonal interleaving as taught by Yi. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a diagonal interleaver for improved performance as taught by Yi (see abstract).

Allowable Subject Matter

10. Claims 6 to 10 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 11 and 19 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter: the instant invention is directed to a decoder for use in a data communication system wherein random and burst errors may be present in the transmitted information code, the decoder comprising an error correction circuit performing error correction on a de-interleaved data by utilizing a first decoding and a second decoding step.

The prior art made of record teaches a decoder for receiving interleaved encoded data, de-interleaving the received data and decoding according to a C1 decoding and a C2 decoding; however, the teaches of the prior art made of record is different form the

instant invention in that the prior art made of record fails to teach or fairly suggest or render obvious the novel element of the error correction circuit within a decoder.

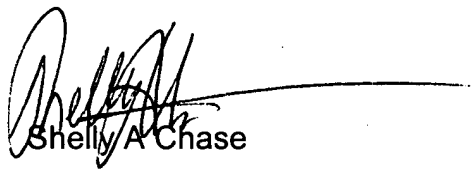
Specifically, the prior art made of record, taken alone or in combination fails to teach or fairy suggest the novel element as recited in the independent claims of a decoder for use in a data communication system comprising an error correction circuit configured to perform a first decoding process and a second decoding process. Claims 12 to 18 and 20 to 24 are directly or indirectly dependent on claims (11 and 19) thus; are allowed over the prior art made of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shelly A Chase